RECEIVER MODULE (VHF)
AT04880/02-04,12-14,22-24

INTRODUCTION

The receiver module converts the RF signals at the antenna into audio which is processed in the control module. Carrier level squelch and noise squelch outputs are also provided to the control module. The injection frequency is derived from an oven controlled oscillator.

DETAILED DESCRIPTION

RF Head.

RF signals at the antenna socket SKA are routed via low-pass filter L33,L24 and C39, C115 to a multi-stage bandpass varicap tuned filter comprising L9-L12 (L9-L11 E Band), CV4-CV7 (CV4-CV6 E Band) and D7-D14 (D7-D12 E Band). The preset variables allow the head response to be optimised over the frequency band in use, while RV2 and RV3 optimise the tracking of the voltage controlled filters. The filtered RF signal is then mixed with the local oscillator signal in the dual-gate mixer TR8.

Crystal Oscillator

A crystal oscillator, TR6 and XL1, operating at 8,4MHz in a fundamental parallel mode, provides the reference frequency and determines the frequency stability of the receiver. The crystal is enclosed in a temperature controlled oven assembly (AT28910/04) which maintains the temperature at 80°C ± 2°C over the temperature range of -30°C to +60°C and provides a stability of ±2ppm. The output of this oscillator is fed to the synthesizer, IC3 on pin 8.

Voltage Controlled Oscillator

TR1 is configured as a voltage controlled oscillator, operating at the final injection frequency, under the influence of coil L1, preset capacitor CV1 and varicaps D1 and D2. Output from the oscillator is amplified by TR3 and split to feed the mixer (via amplifier TR2 and filter L32, CV3, D5 and D6) and the prescaler IC2 (via amplifier TR4).

Synthesizer

Customer channel information is contained within the PROM IC13. Channel selection is achieved by addressing the PROM via the seven parallel address lines C0 to C6 which are connected, via pull-up resistor network RN1 to the 15-way connector.

IC10, a custom EPLD (Electronically programmable logic device) detects the channel change command and instructs the synthesizer to strobe the EPROM for the new channel information.

Channel information is fed from the EPROM to the synthesizer in the form of eight separate four-bit words (D0-D5) on synthesizer pins 11-14. This channel information selects the correct divide ratios in the crystal oscillator and VCO paths, for the frequency requested. The two signals, suitably divided, are then fed to a phase comparator within IC3, the resultant error signals on pin 2 (coarse) and pin 1 (fine) are then filtered and amplified in IC1b, the output of which is used to control the VCO frequency (via D1,D2) and the front-end filter frequency, via IC4a and b, and D7-D14 (D7-D12 E Band). Failure of the receiver to achieve lock is signalled on IC3 pin 3. This illuminates an on-board LED and provides, via TR7, a lock fail alarm to PLA pin 12.

IF Stages

The IF output (21,4MHz) from mixer TR8 is matched by C60, C103, L32 and R56 into crystal filter FL1 which provides the first IF selectivity. L32 and LV2 allow optimisation of the matching to this filter. The filtered output is buffered by TR9, and fed to IC5, which contains an oscillator (controlled by XL2) and mixer, which converts the incoming 21,4MHz signal to the second IF of 455kHz. This is filtered (FL2) and fed to IC6, which further amplifies, limits, and demodulates the signal. Further inter-stage filtering is provided by FL3 which also ensures good metering sensitivity.

IC6 provides a DC signal strength output on pin 5 and the demodulated audio appears on pin 6.

Audio Stages

The demodulated signal from IC6 is amplified by IC7 a,b and c; this stage incorporates some temperature dependent level compensation, and provides a suitable audio output for further processing by the control module; IC7d, IC8a and b filter and amplify the higher-frequency noise components of the signal for use with the noise-operated squelch circuitry within the control module. Gain adjustment of this noise is provided by RV4.

Metering Circuit

The DC level on IC6 pin 5 is dependent upon the incoming RF signal strength. This signal is buffered and amplified by IC9b and d and fed to connector PLA pin 4 for use in the carrier mute circuitry of the control module, and to provide signal strength metering. Thermistor TH2 provides temperature-dependent compensation, whilst RV6 and RV7 provide slope and level offset adjustment respectively.

Regulation

IC12 regulates the incoming 18V down to 14V (adjustable by RV1), whilst IC11 provides a separate 5V supply. The presence of the 14V supply is detected by TR10, the output of which is fed to PLA pin 3 for external monitoring.

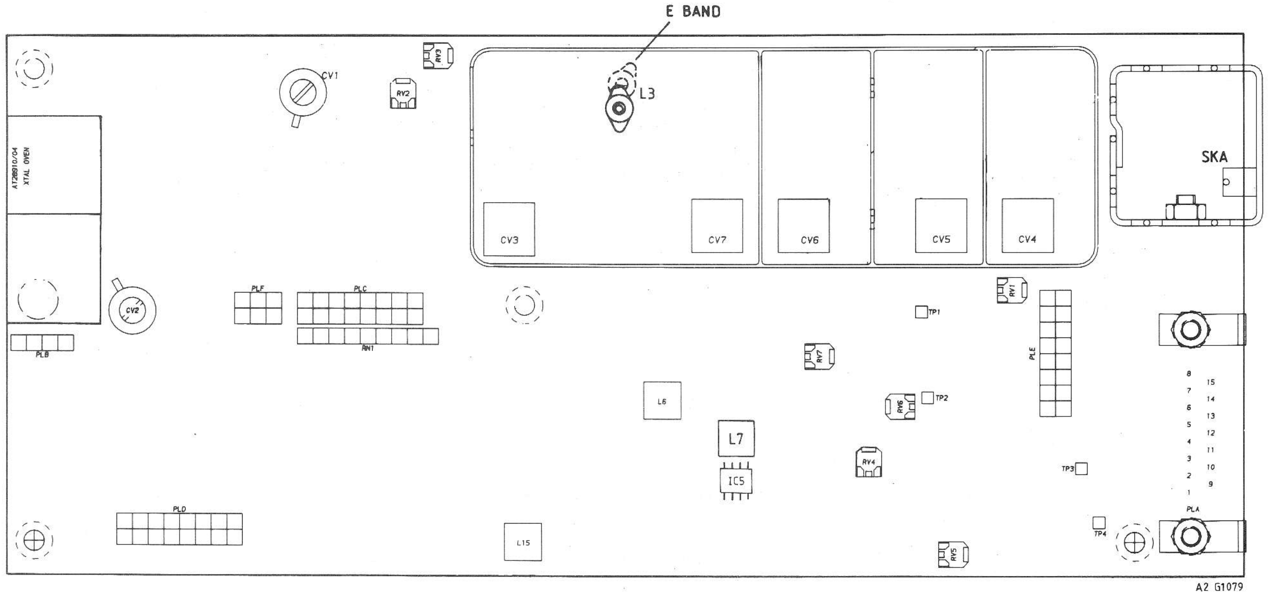


Fig.1 VHF Receiver Alignment Diagram

TEST PROCEDURE (AT04880/02-04,12-14,22-24)

Test Equipment

Item	Description	Requirement	Suitable Type
	Test jig	see Fig.2 of AT04880(UHF)	-
1	Power supply	18V 1A	Kingshill
	Ammeter	50µA, 1A FSD	Select-test 50 or Philips PM2519
	Voltmeter	Very high input impedence, 100kΩ/V min.	Philips PM2519
5	Oscilloscope	general purpose (diagnostic only)	Hamed 203.5
6	SINAD meter	resolution to 0,1%	HP 333A
10	Signal generator	-	HP 8640B
11	Marker oscillator	21,4MHz or 2nd harmonic of 10,7MHz marker.	TCL PT507
	Psophometer	-	HP3556A

Preliminary

1 Set all PCB potentiometers to mid-position and set the Test Jig switches as follows:-

S1 leakage; S2 position 1; S3 position 1; S4 test; S10-16 '0'.

2 Check that an EPROM has been fitted to the Rx module under test.

3 Connect Test Jig and switch on PSU. Check that the chassis leakage current as read by the ammeter is 5µA or less.

4 Adjust RV1 for a voltmeter reading of 14V.

5 Temporarily unplug crystal oven (PLB), set ammeter to 1A FSD and S1 to supply, check that the supply current is 0,2mA or less. Reconnect crystal oven (PLB).

6 Check that the PCB 'lock fail' LED and the Test Jig 'inj fail' LED are illuminated, if necessary adjust CV1. Check that the 'Rx supply volts present' LED on the Test Jig is illuminated.

Synthesiser Alignment

1 Determine the mean of the customer's highest and lowest frequencies, note the PROM test Channel closest to this frequency. This will be the centre channel for alignment purposes unless ±2,25% of this frequency is outside the band edge. In this case use the following as the centre channel:-

A BAND	B BAND	E BAND
149,49MHz	134,97MHz	69,6MHz
169,95MHz	152,46MHz	86MHz

Determine the test channels closest to ±2,25% of the centre channel ('high' and 'low' channels).

2 Set S2 on the Test Jig to position 2, the voltmeter will now show the VCO control voltage. Select the centre channel on the Rx.

3 Adjust CV1 for 6V VCO control voltage, check that the PCB 'lock fail' LED and the 'inj fail' LED on the Test Jig are not illuminated.

4 Select the low channel, check that the VCO voltage is 1,3V minimum.
Select the high channel, check that the VCO voltage is 12V maximum.
If necessary adjust CV1 to meet these conditions.

General Alignment

Note:

(i) All RF levels are in PD

(ii) Unless otherwise stated, modulation is 60% deviation at 1kHz

(iii) On E Band ignore references to CV7.

1 Set the RF signal generator output to 1V, deviation 60% at 1kHz.
Set S3 to position 2 to measure the audio output.
Adjust L15 (discriminator) for maximum output.
Adjust RV5 to give 300mV audio.

2 Set S2 to position 4, the DC voltmeter will now read carrier level volts (RSSI).
Adjust the RF level to give approximately 5V RSSI reading.
Adjust L3, L6 and L7 for maximum RSSI reading.

Note: The crystal oven must have been 'on' for at least 5 minutes before carrying out the following check.

3 Select the centre channel on the Rx and signal generator, switch off the modulation. Set S3 to position 2, adjust the RF level and observe quieting on the oscilloscope, if quieting is not observed, even with 1V RF level, adjust crystal trimmer CV2.
Hold the 21,4MHz marker oscillator close to IC5 and adjust CV2 for 'zero beat' on the oscilloscope.

4 Set S2 to position 2; DC voltmeter will now read RF head voltage, from the appropriate graph determine the required head voltage for the centre channel. Adjust RV2 (and RV3 if necessary) to obtain this voltage.

5 Set S3 to position 1 (de-emphasis on), switch on the modulation. Set the distortion analyser to measure SINAD with CCITT weighting; adjusting the RF level as necessary, adjust CV3, CV7, CV6, CV5 and CV4 for best SINAD until no further improvement is possible.

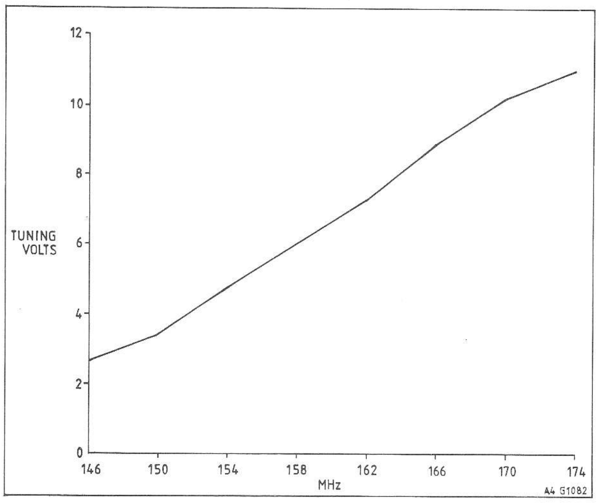
6 Set S2 to position 4 (RSSI), adjust RF level to give approximately 5V RSSI reading. Adjust CV3 for maximum RSSI level. Check that the SINAD with 0,5μV RF level is at least 20dB.

7 Adjust the RF level to give 20dB SINAD, set S3 to position 3 and measure the noise level. Adjust RV4 to give 100mV of noise.

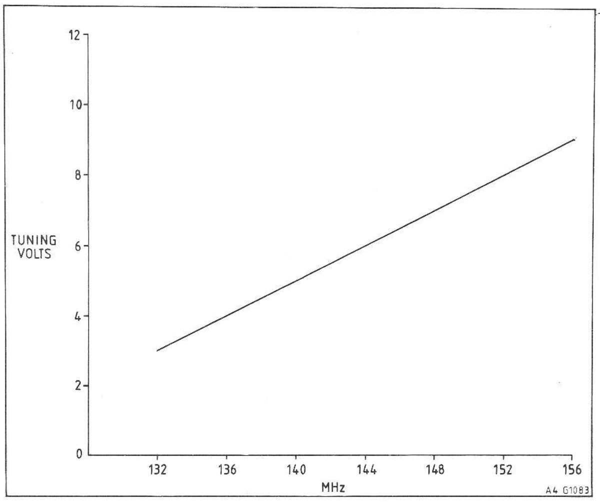
8 Set the RF signal generator to give 1mV modulated output, set S3 to position 1 and measure the distortion without CCITT weighting. On 12,5kHz and 20kHz channel spacing equipments only adjust L6 for minumum distortion.

9 Set S2 to position 4 (RSSI), with 0,3µV RF input adjust RV7 to give 4V RSSI. Increase RF level to 30µV; if RSSI voltage is less than 10V adjust RV6 clockwise, if RSSI voltage is greater than 10V adjust RV6 counter-clockwise. Adjust RV6 and RV7 until 4V and 10V RSSI are obtained for RF levels of 0,3µV and 30µV respectively.

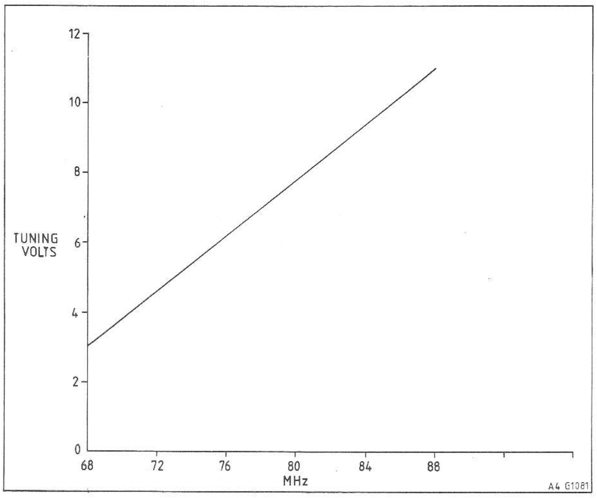
10 Set S3 to position 2, with an RF input of 1mV modulated, note the audio output level on the dB scale (0dB reference).
Set the modulating frequency to 300Hz and check that the audio level is within ±0,5dB.
Set the modulating frequency to 3kHz and check that the audio level is within ±0,5dB.



A Band RF Head Tuning



B Band RF Head Tuning



E Band RF Head Tuning

Front-end Tracking

1 Set S2 to position 3 (head volts) and S3 to position 1 (de-emphasis on), record head voltage on centre channel. Select low channel on Test Jig and RF signal generator, set RF input to 0,5µV modulated. Switch on CCITT weighting.

2 Adjust RV2 (and if necessary RV3) for best SINAD, record head voltage.

3 Repeat step 2 but with the high channel.

4 Adjust RV2 and RV3 so that the voltage noted in steps 2 and 3 are obtained when the low and high channels are selected.

5 Select the centre channel on the Test Jig, compare the head voltage with that noted in step 1. If there is more than 0,3V difference adjust RV2 to halve the error.

6 Check that the SINAD on all three channels is 20dB minimum.

VHF RECEIVER ADJUSTMENTS

The following is a list of the tunable components within the unit together with the parameter for which they are adjusted;

Component	**Parameter**
RV1	Set for 14V on TP1
RV2	Front-end tracking offset — Refer to alignment procedure.
RV3	Front-end tracking gain — Refer to alignment procedure.
RV4	Set for 100mV noise on TP3 with RF level set to give 20dB psophometric SINAD.
RV5	Audio level. Set for 300mV audio on TP4 with 1mV RF level, modulation 60% at 1kHz.
RV6	RSSI slope — Set for DC levels on TP2: 4V for 0,3µV RF level. 10V for 30µV RF level.
RV7	RSSI gain — Set for DC levels on TP2: 4V for 0,3µV RF level. 10V for 30µV RF level.
CV1	VCO trimmer. Set for 6V DC on PLF pin 6 on centre channel.
CV2	Crystal oscillator. Set for zero beat with marker oscillator.
CV3	Injection filter. Adjust for maximum DC level on TP2 with RF level set to give approximately 5V on TP2.

Component	Parameter
CV4-6 CV7 (A/B Band only)	RF front-end. Refer to alignment procedure.
L3 L7	1st IF. Adjust for maximum DC level on TP2 with RF level set to give approximately 5V on TP2.
L6	1st IF. Adjust for lowest distortion (12,5 and 20kHz channel spacing) with 1mV RF level, modulation 60% at 1kHz. On 25kHz channel spacing adjust for maximum DC level on TP2 with RF level set to give approximately 5V on TP2.
L15	Discriminator coil. Adjust for maximum audio level on TP4 with 1mV RF level, modulation 60% at 1kHz.