RECEIVER MODULE (UHF)
AT04880/05-07,15-17,25-27

INTRODUCTION

The receiver module converts the RF signals at the antenna into audio which is processed in the control module. Carrier level squelch and noise squelch outputs are also provided to the control module. The injection frequency is derived from an oven controlled crystal oscillator.

DETAILED DESCRIPTION

RF Head

RF signals at the antenna are routed via low-pass filter L1,L2 and C1 to a two-stage bandpass varicap tuned filter comprising L3, L4, C6-C14 and D1-D8. RF amplification is provided by TR1, the output of which is fed to a further four stages of varicap tuned bandpass filtering L4, L6-L8, D9-D24 and C20-C48. Preset variables C6, C14, C20, C30, C38 and C47 allow the head response to be optimised over the frequency band in use. RV2 and RV3 optimise the tracking of the voltage controlled filters and oscillator.

Crystal Oscillator

A crystal oscillator, TR9 and XL2, operating at 8,4MHz in a fundamental paralled mode, provides the reference frequency and determines the frequency stability of the receiver. The crystal is enclosed in a temperature-controlled oven assembly (AT28910/04) which maintains the temperature at 80°C ±2°C over the temperature range of -30°C to +60°C, and provides a stability of ±2ppm. The output of this oscillator is fed into the synthesizer, IC11, on pin 8.

Voltage Controlled Oscillator

TR4 is configured as a voltage controlled oscillator, operating at the final injection frequency, under the influence of the ¼-wavelength dielectric resonator CR1, preset capacitor C95 and varicap diode D26. Output from the oscillator is amplified by TR5 and then fed via TR9 to the mixer, and via TR6 to the prescaler IC9 and onwards to synthesizer IC11.

Synthesizer

Customer channel frequency information is contained within the PROM, IC13. Channel selection is achieved by addressing the PROM via the 7 parallel address lines C0 to C6 which are connected, via pull-up resistor network RN1 to the 15-way supply connector.

IC12, a custom EPLD (Electronically programmable logic device) detects any channel change and instructs the synthesizer to strobe the EPROM for the new channel information.

Channel information is fed from the EPROM to the synthesizer in the form of eight separate four-bit words (D0-D3) on synthesizer pins 11-14. This channel information selects the correct divide ratios in the crystal oscillator and VCO input paths, for the frequency requested. The two signals, suitably divided, are then fed to a phase comparator within IC11, the resultant error signals on pin 2 (coarse) and pin 1 (fine) are then filtered and amplified in IC8, the output of which is used to control the VCO frequency (via D26) and the front-end filter frequency (via IC1, RV2, RV3 and D9-D24). Failure of the receiver to achieve lock is signalled on IC11 pin 3. This illuminates on-board LED1 and provides, via TR11, a lock fail alarm to PLA pin 12.

IF Stages

The RF signal from the RF head is mixed with the buffered VCO output in the RMS1 mixer. The IF output of the mixer (21,4MHz) is stepped up in impedance (L9,C49, C50) and applied to dual-gate FET amplifier TR2. FL1, a crystal filter, provides the first IF selectivity. Preset controls L11, L12 and C58 allow optimisation of the matching to this filter. IC4 contains an oscillator (controlled by XL1) and mixer, which converts the incoming 21,4MHz signal to the second IF of 455kHz. This is then filtered (FL2) and fed to IC5, which further amplifies, limits and demodulates the signal. Further inter-stage filtering is provided by FL3 and ensures a good metering sensitivity.

IC5 provides a DC signal strength output on pin 5 and the demodulated audio appears on pin 6.

Audio Stages

The demodulated signal from IC5 is amplified by IC6; this stage incorporates some temperature-dependent level compensation. The audio signal is then split, IC14 and RV5 providing a suitable audio output for further processing by the control module; IC14 and IC15 filtering and amplifying the higher-frequency noise components of the signal for use with the noise-operated squelch circuitry within the control module. Gain adjustment of this noise is provided by RV6.

Metering Circuit

The DC level on IC5 pin 5 is dependent upon the incoming RF signal strength. This signal is buffered and processed by IC8 and fed to connector PLA pin 4 for use in the carrier mute circuitry of the control module, and to provide signal strength metering. Thermistor R99 provides temperature-dependent compensation, whilst RV7 and RV8 provide level shift and slope adjustment.

Regulation

IC7 regulates the incoming 18V down to a 14V (adjustable by RV1), whilst IC3 and IC10 provide separate internal 5V supplies. The presence of the 14V supply is detected by TR8 the output of which is fed to PLA pin 3 for external monitoring.

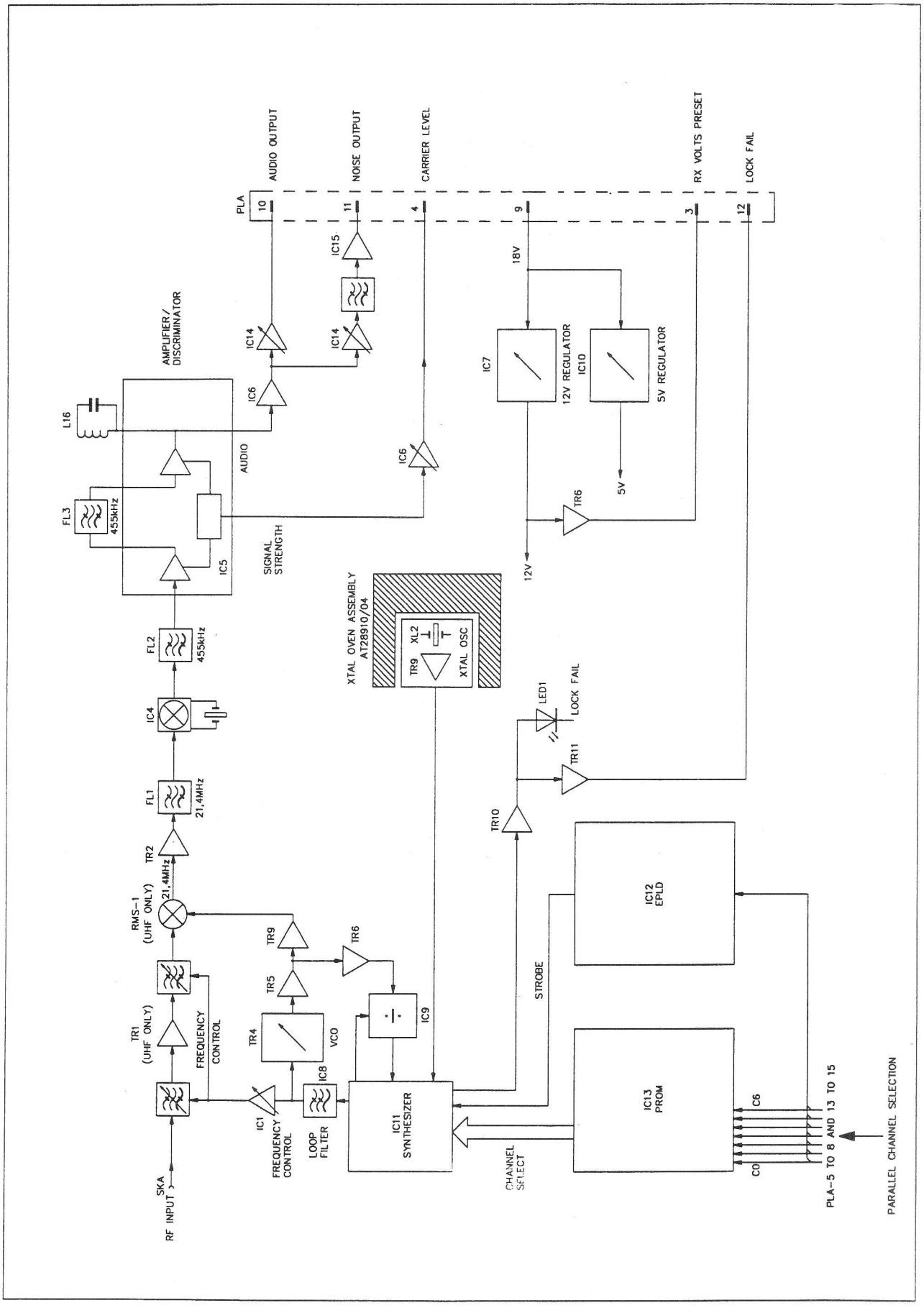

Fig.1 Rx Block Diagram AT04880/-

TEST PROCEDURE (AT04880/05-07, 15-17, 25-27)

Note:

The following test procedure, which should not be attempted without the specified test equipment, is for full alignment of the unit to ex-factory standard; re-tuning to this level should not normally be required in the field.

Test Equipment

Item	Description	Requirement	Suitable Type
	Test jig	see Fig.2	-
1	Power supply	18V 1A	Kingshill
	Ammeter	50µA, 1A FSD	Select-test 50 or Philips PM2519
	Voltmeter	Very high input impedence, 100kΩ/V min.	Philips PM2519
5	Oscilloscope	general purpose (diagnostic only)	Hamed 203.5
6	SINAD meter	resolution to 0,1%	HP 333A
10	Signal generator	-	HP 8640B
11	Marker oscillator	21,4MHz or 2nd harmonic of 10,7MHz marker.	TCL PT507
	Psophometer	-	HP3556A

1 **Preliminary**

(a) Set all PCB pots to mid-range, and the test jig switches S1 to leakage, S2 to position 1, S3 to position 1, S4 to test, S10-16 to '0'.

(b) Check that an EPROM (memory) IC has been fitted to the PCB under test. Note that all EPROMS blown to spec AT60171 have, in addition to any customer information, a set of 128 test frequencies blown into them, and that testing is accomplished using these test frequencies (see Table 1 for frequency listing).

(c) Connect the unit to be tested to the test jig, and with the PSU switched on, check the chassis leakage current as measured by the ammeter is no greater than 5µA

(d) Set the ammeter to 1A FSD, and set S1 to 'supply', check that the ammeter reading is no greater than 0,4A.

(e) Connect the voltmeter probe to TP1, and adjust RV1 for a voltmeter reading of 14V.

(f) Check that the PCB 'lock fail' LED and the test jig 'lock fail' and 'Rx supply volts present' LEDs are all lit.

2 Synthesizer alignment

(a) From customer information, determine the highest receiver frequency and set switches S10-16 on the test jig to the next highest test channel frequency, as indicated in Table 1. If no customer information is available, select a test channel equivalent to the top band edge frequency.

(b) Set S2 on the test jig to position 2. The voltmeter will now read the synthesizer loop control voltage.

(c) Adjust the multiturn VCO trimmer C95 through its range until the PCB 'lock fail' LED extinguishes. Check that the test jig 'lock fail' LED is also extinguished. The synthesizer is now in lock.

(d) As the VCO trimmer is adjusted within lock, the reading on the voltmeter will change. Adjust for a 12V reading.

(e) Reset test jig switches S10-16, to the channel twenty lower (see paragraph 2(f) if this is not possible). Check voltmeter reading is between 2V and 5V.

(f) If paragraph 2(e) would require selecting a channel lower than 0, set to channel 0. Check voltmeter reading is 2V minimum.

(g) Check that the test jig 'lock fail' LED is still extinguished.

(h) Reset switches S10-16 to produce original channel [as paragraph 2(a)], and S2 on the test jig set to position 3, the voltmeter will now read the head volts.

(j) Adjust RV2 for a voltmeter reading of 12V.

3 General alignment

(a) Ensure that the receiver has been switched on for at least two minutes before this check is attempted.

Set the signal generator to the required frequency with no modulation. Increase the generator level until the 'scope indicates that the receiver is 'quieting'. If, even with 1V output, quieting is not observed, adjust the multiturn trimmer C177 until it is found. Net the receiver onto channel using the 21,4MHz marker by adjusting C177 for zero beat.

(b) Apply 1kHz modulation at 60% system deviation, and adjust trimmers C6, 14,20,30,38 and 47 for the best SINAD, reducing the generator output as necessary. Likewise, adjust L9 for best SINAD.

(c) Increase the signal generator output by 60dB, and adjust L11, L12 and C58 for best SINAD, minimum value 35dB.

(d) Reset the signal generator output level to 0,3µV and re-measure the SINAD (psophometrically), minimum value 20dB.

(e) Set S3 to position 2, and adjust RV5 on the PCB to produce a distortion analyser voltmeter reading of 300mV.

(f) Set S3 to position 3 and set the generator level to give 20dB psophometric SINAD, adjust RV6 on the PCB to produce a distortion analyser voltmeter reading of 100mV.

(g) Set S2 on the test jig to position 4, the voltmeter will now read carrier level volts.

(h) With the signal generator frequency still off channel, set RV8 to mid-travel and adjust RV7 for maximum voltmeter reading.

(j) Return the signal generator frequency onto channel frequency at a level of 0,3µV. Adjust RV8 for a voltmeter reading of 4V.

(k) Set the signal generator level to zero and check that the voltmeter reading is no greater than 3,3V.

(l) Set the signal generator level to 10µV and check that the voltmeter reading is between 7,5V and 8,8V

4 Front-end Tracking

(a) Set the receiver to the highest frequency channel as in paragraph 2(a).

(b) Set S2 on the test jig set to position 2, check that the voltmeter reads 12V. (adjust C95 slightly, if required).

(c) Reset the test jig switches S10-16 to the channel twenty lower, as in paragraph 2(e), and set the signal generator to this channel frequency.

(d) Adjust RV3 for best SINAD, and with the generator output set to 0,5µV, measure the SINAD (psophometrically), minimum value 20dB.

(e) Return the receiver and signal generator to the channel and frequency indicated in paragraph 4(a), reset RV2, if necessary, for best SINAD, with the generator output at 0,5µV measure the SINAD (psophometrically), minimum value 20dB.

(f) Repeat paragraph 4(d).

(g) Set S4 on the test jig to 'customer', and check that the psophometric SINAD (for a generator level of 0,5µV) for all customer channels is 20dB minimum.

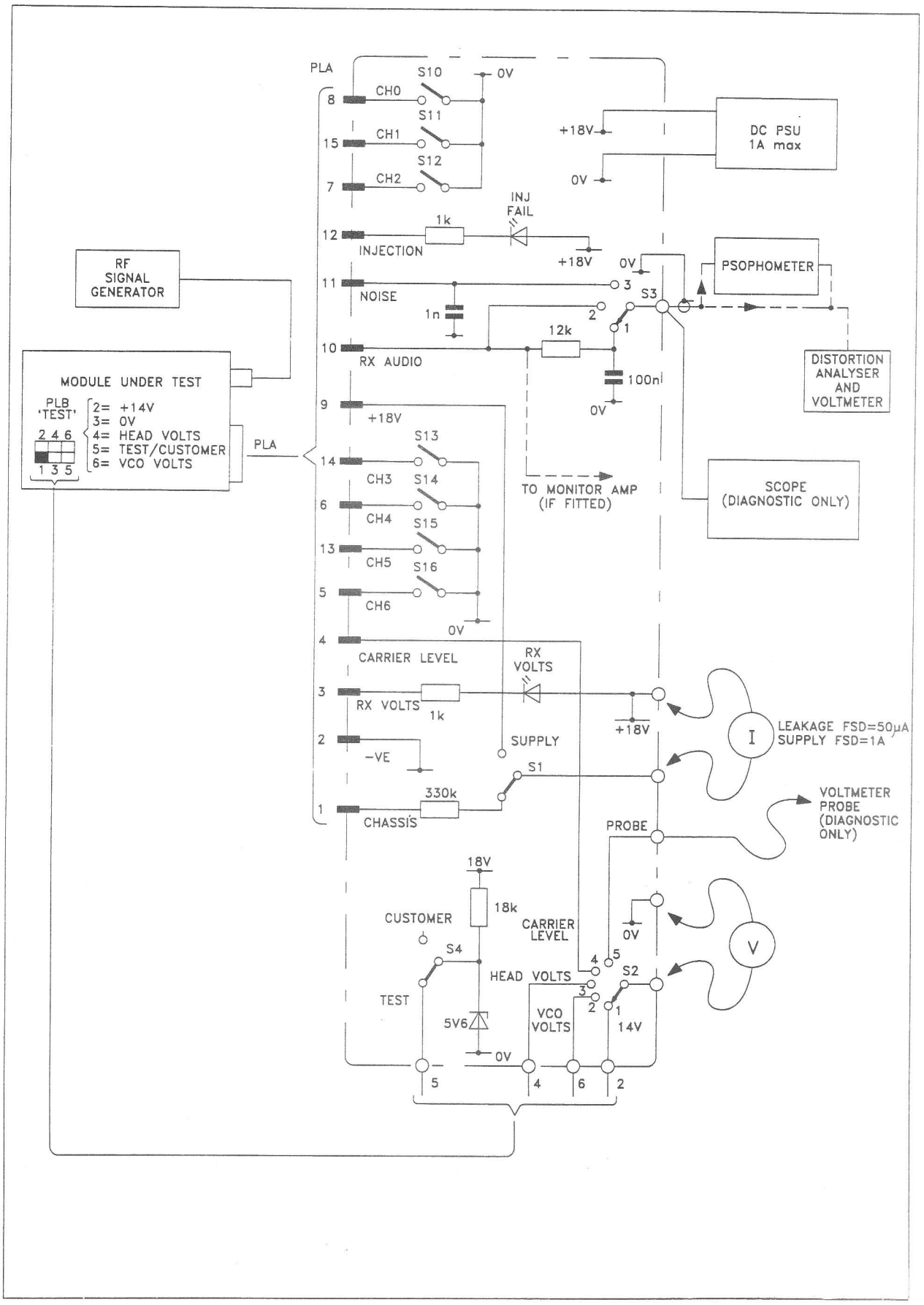

Fig.2 Test Jig

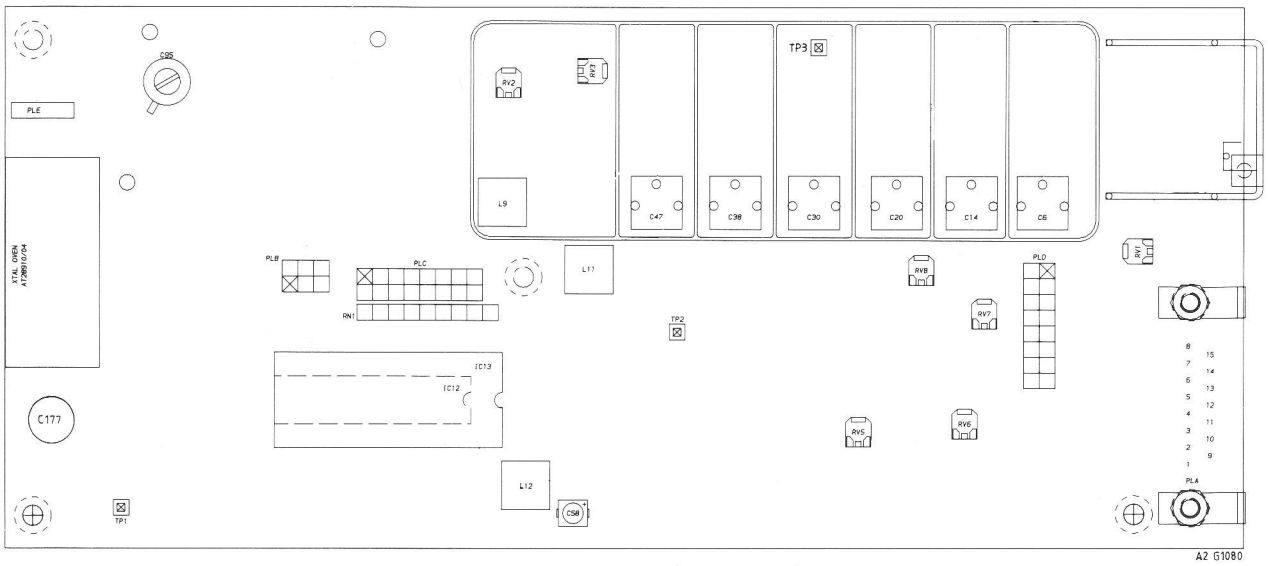

Fig.3 UHF Receiver Alignment Diagram