74196 276-1833 40 MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

GENERAL DESCRIPTION

These high-speed monolithic counters consist of four dc coupled master/slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter. These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 40 MHz at the clock 1 input and 0 to 20 MHz at the clock 2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission line effects and simplify system design. The circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 150 mW.

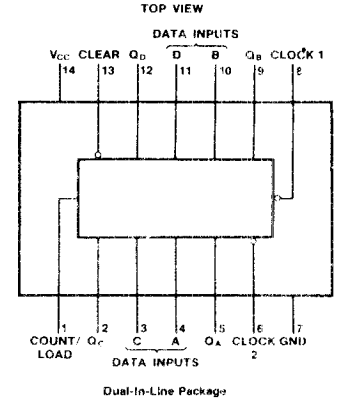
FEATURES

- Performs BCD, bi-quinary, or binary counting
- Fully independent clear input
- Guaranteed to count at input frequencies from 0 to 40 MHz
- Input clamping diodes simplify system design

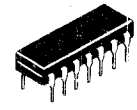
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 5.25V
Input Voltage 5.5V
Interemitter Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage (V_{CC}) ..... 4.75—5.25V
Temperature (T_A) ..... 0°C to 70°C

PIN CONNECTION



Dual-In-Line Package



TRUTH TABLES

DECADE (BCD)
74196 (Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
74196 (Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A: Output Q_A connected to clock 2 input.

Note B: Output Q_D connected to clock 1 input.

LOGIC DIAGRAM